WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor element comprising:

forming a gate insulating film over a semiconductor region;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming an insulating film covering the gate electrode;

exposing a part of the semiconductor region;

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region;

forming a resist over the conductive film;

removing a portion of the resist to form a resist mask;

etching a part of the conductive film by using the resist mask; and

etching a part of the etched conductive film.

2. A method for manufacturing a semiconductor element comprising:

forming a gate insulating film over a semiconductor region;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming an insulating film covering the gate electrode;

exposing a part of the semiconductor region;

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region;

forming a resist over the conductive film;

removing a portion of the resist to form a resist mask;

etching a part of the conductive film by using the resist mask; and

etching a part of the etched conductive film and a part of the semiconductor region.

3. A method for manufacturing a semiconductor element comprising:

forming a gate insulating film over a semiconductor region;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

exposing a part of the semiconductor region;

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region;

etching a part of the conductive film;

forming a resist over the conductive film;

removing a portion of the resist to form a resist mask; and

etching a part of the conductive film by using the resist mask.

4. A method for manufacturing a semiconductor element comprising:

forming a gate insulating film over a semiconductor region;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

exposing a part of the semiconductor region;

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region;

etching a part of the conductive film and a part of the semiconductor region;

forming a resist over the conductive film;

removing a portion of the resist to form a resist mask; and

etching a part of the conductive film by using the resist mask.

5. A method for manufacturing a semiconductor element comprising:

forming a first insulating film over a semiconductor region;

forming a first conductive film over the first insulating film;

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode;

forming a third insulating film over the semiconductor region;

etching the third insulating film to form a sidewall;

etching the first insulating film by using the sidewall and the hard mask as a mask to form a gate insulating film;

exposing a part of the semiconductor region;

forming a second conductive film;

forming a resist over the second conductive film;

removing a portion of the resist to form a resist mask;

etching a part of the second conductive film by using the resist mask as a mask; and

etching a part of the etched second conductive film and a part of the semiconductor region to form a source and drain electrode.

6. A method for manufacturing a semiconductor element comprising:

forming a first insulating film over a semiconductor region;

forming a first conductive film over the first insulating film;

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode;

forming a third insulating film over the semiconductor region;

etching the third insulating film to form a sidewall;

etching the first insulating film by using the sidewall and the hard mask as a mask to form a gate insulating film;

exposing a part of the semiconductor region;

forming a second conductive film;

etching a part of the second conductive film;

forming a resist over the second conductive film;

removing a portion of the resist to form a resist mask; and

etching a part of the second conductive film by using the resist mask as a mask to form a source and drain electrode.

7. A method for manufacturing a semiconductor element according to Claim 1, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

8. A method for manufacturing a semiconductor element according to Claim 1, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film.

9. A method for manufacturing a semiconductor element according to Claim 1, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

10. A method for manufacturing a semiconductor element according to Claim 9, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

11. A method for manufacturing a semiconductor element according to Claim 9, wherein the semiconductor thin film is a crystalline silicon film.

12. A method for manufacturing a semiconductor element according to Claim 2, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

13. A method for manufacturing a semiconductor element according to Claim 2, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film.

14. A method for manufacturing a semiconductor element according to Claim 2, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

15. A method for manufacturing a semiconductor element according to Claim

14, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

16. A method for manufacturing a semiconductor element according to Claim 14, wherein the semiconductor thin film is a crystalline silicon film.

17. A method for manufacturing a semiconductor element according to Claim 3, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

18. A method for manufacturing a semiconductor element according to Claim 3, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film.

19. A method for manufacturing a semiconductor element according to Claim 3, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

20. A method for manufacturing a semiconductor element according to Claim 19, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

21. A method for manufacturing a semiconductor element according to Claim 19, wherein the semiconductor thin film is a crystalline silicon film.

22. A method for manufacturing a semiconductor element according to Claim 4, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

23. A method for manufacturing a semiconductor element according to Claim 4, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film.

24. A method for manufacturing a semiconductor element according to Claim 4, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

25. A method for manufacturing a semiconductor element according to Claim 24, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

26. A method for manufacturing a semiconductor element according to Claim 24, wherein the semiconductor thin film is a crystalline silicon film.

27. A method for manufacturing a semiconductor element according to Claim 5, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

28. A method for manufacturing a semiconductor element according to Claim 5, wherein the resist mask is formed by etching an entire face of the resist, and exposing a

part of the second conductive film.

29. A method for manufacturing a semiconductor element according to Claim 5, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

30. A method for manufacturing a semiconductor element according to Claim 29, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

31. A method for manufacturing a semiconductor element according to Claim 29, wherein the semiconductor thin film is a crystalline silicon film.

32. A method for manufacturing a semiconductor element according to Claim 6, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

33. A method for manufacturing a semiconductor element according to Claim 6, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the second conductive film.

34. A method for manufacturing a semiconductor element according to Claim 6, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

35. A method for manufacturing a semiconductor element according to Claim 34, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

36. A method for manufacturing a semiconductor element according to Claim 34, wherein the semiconductor thin film is a crystalline silicon film.

37. A semiconductor element comprising:

a semiconductor region having a source region, a drain region, and a channel forming region;

a gate electrode;

a gate insulating film;

a contact portion for connecting the semiconductor region to a source and drain electrode; and

an insulating film covering the gate electrode,

wherein between the channel forming region and the contact portion is from 0.2 μm to 0.5 μm.

38. A semiconductor element comprising:

a semiconductor region having a source region, a drain region, and a channel forming region;

a gate electrode;

a gate insulating film;

a contact portion for connecting the semiconductor region to a source and drain electrode; and

wherein the gate electrode and the source and drain electrode are formed with the insulating film covering the gate electrode therebetween.

39. A semiconductor element according to Claim 37, wherein the insulating film covering the gate electrode comprises an insulating film that is formed over the gate electrode and an insulating film that is formed in a side face of the gate electrode.

40. A semiconductor element according to Claim 38, wherein the insulating film covering the gate electrode comprises an insulating film that is formed over the gate electrode and an insulating film that is formed in a side face of the gate electrode.

41. A semiconductor element according to Claim 37, wherein the insulating film that is formed over the gate electrode is a hard mask and the insulating film that is formed in a side face of the gate electrode is a sidewall.

42. A semiconductor element according to Claim 38, wherein the insulating film that is formed over the gate electrode is a hard mask and the insulating film that is formed in a side face of the gate electrode is a sidewall.

43. A semiconductor element according to Claim 37, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

44. A semiconductor element according to Claim 38, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

45. A semiconductor element according to Claim 43, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

46. A semiconductor element according to Claim 44, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

47. A semiconductor element according to Claim 43, wherein the semiconductor thin film is a crystalline silicon film.

48. A semiconductor element according to Claim 44, wherein the semiconductor thin film is a crystalline silicon film.

49. A method for manufacturing a semiconductor device having a method for manufacturing a semiconductor element according to Claim 1.

50. A method for manufacturing a semiconductor device having a method for manufacturing a semiconductor element according to Claim 2.

51. A method for manufacturing a semiconductor device having a method for manufacturing a semiconductor element according to Claim 3.

52. A method for manufacturing a semiconductor device having a method for manufacturing a semiconductor element according to Claim 4.

53. A method for manufacturing a semiconductor device having a method for manufacturing a semiconductor element according to Claim 5.

54. A method for manufacturing a semiconductor device having a method for manufacturing a semiconductor element according to Claim 6.

55. A semiconductor device comprising a semiconductor element formed according to Claim 37.

56. A semiconductor device comprising a semiconductor element formed according to Claim 38.